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APPLICATION FOR LETTERS PATENT

TITLE: DIGITAL STEREO DEMULTIPLEXER

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Description

1 The present invention relates to the demultiplexing of a frequency demodulated stereo-multiplex signal.

In fm-broadcasting a stereo-multiplex signal is frequency modulated. The ste-
5 reo-multiplex signal consists of a stereo-sum signal and a stereo-difference signal. The stereo-difference signal is amplitude modulated with suppressed carrier. To allow a coherent amplitude demodulation of the stereo-difference signal at the receiver, a pilot carrier with half the AM-carrier frequency is added to the stereo-multiplex signal.

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The stereo-sum signal and the stereo-difference signal are defined by

$$m_s(t) = a_l(t) + a_r(t)$$
$$m_d(t) = a_l(t) - a_r(t)$$

15 wherein $a_l(t)$ is the signal of the left audio channel and $a_r(t)$ is the signal of the right audio channel.

The stereo-multiplex signal is defined by

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$$m_{stmux}(t) = m_s(t) + \sin(2\,\omega_{pil}t) \cdot m_d(t) + A_{pil} \cdot \sin(\omega_{pil}t)$$

wherein ω_{pil} is the carrier frequency and A_{pil} is the amplitude of the carrier.

25 The stereo-multiplex signal is frequency modulated:

$$S_{FM}(t) = A_{FM}\cos\left(\omega_c(t) + \Delta\omega \int_{-\infty}^{t} m_{stmux}(\tau)\,d\tau\right)$$

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with ω_c: carrier frequency
    $\Delta\omega$:   frequency deviation

At the receiver side the frequency modulated stereo-multiplex signal is fre-
quency demodulated and stereo-demultiplexed to calculate the left and right

1   audio signal.

For the stereo demultiplexing, the stereo demultiplexer needs to recover the 2nd harmonic of the pilot carrier. Therefore, the pilot carrier is separated from the

5   frequency demodulated stereo-multiplex signal m(t) by a bandpass filter and a PLL locks to the separated pilot carrier and generates the 2nd harmonic of the pilot carrier. The 2nd harmonic, that is locked in phase to the pilot carrier is needed for the coherent amplitude demodulation of the stereo-difference signal.

10 Figure 3 shows the basic functionality of a state of the art stereo demultiplexer. The received frequency modulated stereo-multiplex signal $S_{FM}(t)$ is input to a frequency demodulator 17. The frequency demodulator 17 outputs the frequency demodulated stereo-multiplex signal m(t) that corresponds to the stereo-multiplex signal $m_{stmux}(t)$ as generated on the transmitter side. On basis of this ste-

15 reo-multiplex signal m(t) a PLL-circuit 19 with preceding bandpass filter 18 generates the 2nd harmonic of the pilot carrier, i. e. a signal $2 \cdot \sin(2\omega_{pil}t)$, which is needed for the coherent amplitude demodulation of the stereo-multiplex signal m(t) to gain the stereo-difference signal $m_d(t)$.

20 The coherent amplitude demodulation is performed by way of a demodulator 1 which receives the stereo-multiplex signal m(t) at its first input and the 2nd harmonic of the pilot carrier at its second input. The output signal of the demodulator 1 is input to a filter 20 which outputs the stereo-difference signal $m_d(t)$.

25 The stereo-sum signal $m_s(t)$ is generated by a lowpass filtering of the stereo-multiplex signal m(t) with a lowpass filter 21 that receives the output signal of the frequency demodulator 17.

The left audio signal is calculated by an addition of the stereo-sum signal $m_s(t)$

30 and the stereo-difference signal $m_d(t)$ with an adder 3. The right audio signal r(t) is calculated by a subtraction of the stereo-difference signal $m_d(t)$ from the stereo-sum signal $m_s(t)$ with a subtracter 6.

Therefore, the stereo-sum signal $m_s(t)$ is generated by a lowpass filtering of the

35 stereo-multiplex signal m(t) and the stereo-difference signal $m_d(t)$ is generated by a coherent amplitude demodulation of the amplitude modulated stereo-difference signal. The left and right audio signals l(t) and r(t) are calculated by addi-

1   tion and subtraction of the stereo-sum signal and the stereo-difference signal:

$$r(t) = m_s(t) - m_d(t) = (a_l(t) + a_r(t)) - (a_l(t) - a_r(t)) = 2a_r(t)$$
$$l(t) = m_s(t) + m_d(t) = (a_l(t) + a_r(t)) + (a_l(t) - a_r(t)) = 2a_l(t)$$

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In a digital frequency demodulator the frequency demodulation needs to be performed at a high sampling rate because the bandwidth of the frequency modulating signal is about

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$$B_{fm} = 2(\Delta F + 2f_{nf})$$

with ΔF being the frequency deviation and f_{nf} being the modulation frequency.

From this equation follows that the bandwidth of the frequency modulating
15   signal is much larger than the bandwidth of the modulating signal. Therefore, the frequency demodulated signal can be sampling rate decimated.

Furtheron, the bandwidth of the stereo-multiplex signal is larger than the bandwidth of the audio signal. This can easily be seen in the above equation
20   which defines the stereo-multiplex signal $m_{stmux}(t)$. Therefore, the sampling rate can be reduced in the stereo demultiplexer.

The digital stereo demultiplexer shown in Fig. 4 differs to that shown in Fig. 3 in that the filter 20 and the lowpass filter 21 are replaced by a first sampling
25   rate decimation filter 22 which comprises a digital filter for the generation of the stereo-difference signal $m_d(t)$ and a second sampling rate decimation filter 23 which comprises a digital lowpass filter for the generation of the stereo-sum signal $m_s(t)$. Both sampling rate decimation filters have a decimation factor of D.
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This solution has the disadvantage that the DPLL 19, which works similar to the PLL 19 shown in Fig. 3, needs to run at a high sampling rate. This requires high calculation power and therefore a high power consumption of the DSP that realizes the stereo demultiplexer.
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The DPLL can also work at a reduced sampling rate. A simple method is to reduce the sampling rate of the bandpass filter output signal and to

1 interpolate the DPLL output signal.

Fig. 5 shows such a digital stero-demultiplexer comprising a digital PLL-circuit 25 which works at a reduced sampling rate. In this stereo demultiplexer the generation of the stereo-difference signal $m_d(t)$ and the stereo-sum signal $m_s(t)$

5 is identical as in the stereo demultiplexer shown in Fig. 4, only the generation of the 2nd harmonic of the pilot carrier differs.

The bandpass filter 18 shown in Figs. 3 and 4 is replaced with a third sampling rate decimation filter 24 which comprises a digital bandpass filter. The third

10 sampling rate decimation filter 24 has a sampling rate decimation factor E. The DPLL 25 works with the reduced sampling rate and therefore receives the output signal of the third sampling rate decimation filter 24.

The coherent amplitude demodulation of the stereo-difference signal $m_d(t)$

15 needs to be performed at a sampling rate which is higher than the sampling rate of the audio signal, since the bandwidth of the stereo-multiplex signal m(t) is higher than the bandwidth of the audio signal. Therefore, the carrier for the coherent amplitude demodulation of the stereo-difference signal $m_d(t)$ needs to be generated with a higher sampling rate.

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Fig. 5 shows that the output signal of the digital PLL-circuit 25 is interpolated in an interpolation unit 26 with an interpolation factor of E so that the 2nd harmonic of the carrier is generated with a sampling rate that equals to the sampling rate of the stereo-multiplex signal m(t). Thereafter, to perform the co-

25 herent amplitude demodulation which is necessary to generate the stereo-difference signal $m_d(t)$, the so generated carrier with a carrier frequency of $2\omega_{pil}$ that is locked in phase to the pilot carrier is multiplied with the stereo-multiplex signal m(t) by the demodulator 1.

30 In this embodiment the DPLL 25 runs at a reduced sampling rate and therefore outputs a lower number of samples per sample of the stereo-multiplex signal than the DPLL 19 shown in Fig. 4. So the required calculation power is low. On the other hand, the decimation bandpass filter within the third sampling rate decimation filter 24 and the interpolation bandpass filter within the interpola-

35 tion unit 26 require high calculation power.

Therefore, all described stereo demultiplexers have the particular disadvantage

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1 that a quite high calculation power is needed.

Therefore, it is the object of the present invention to provide a stereo demultiplexer needing less calculation power.

5 The stereo demultiplexer according to the present invention is defined in independent claim 1. Preferred embodiments thereof are defined in dependent claims 2 to 9.

According to the present invention the second sampling rate decimation filter,
10 i.e. the sampling rate decimation filter in the sum path, is used for the sampling rate decimation to generate the 2nd harmonic or any other harmonic of the pilot carrier. This sampling rate decimation filter is available anyway and therefore the sampling rate decimation of the pilot carrier can be performed without an additional filter.
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The sampling rate of the DPLL output signal needs to be upconverted to a higher sampling rate. Therefore, the sampling rate of the DPLL output signal needs to be interpolated by the same factor D than the sampling rate decimation of the stereo-sum signal.
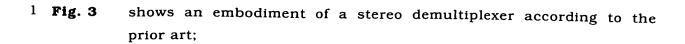20

Preferrably, the sampling rate interpolation of the DPLL output signal is performed in the DPLL without any interpolation filter. In this case the interpolation is achieved on basis of one calculated and D-1 predicted sampling values for the respective harmonic of the pilot carrier. Each of the predicted values is
25 preferrably calculated on basis of a phase correction of the one calculated value which is determined in accordance with the neccessary number of predicted values.

The present invention and its embodiments will be better understood from a de-
30 tailed description of an exemplary embodiment thereof described in conjunction with the accompanying drawings, wherein

Fig. 1   shows a stereo demultiplexer according to a preferred embodiment of the present invention;
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Fig. 2   shows parts of a digital PLL-circuit shown in Fig. 1;

1 **Fig. 3**   shows an embodiment of a stereo demultiplexer according to the
                  prior art;

   Fig. 4   shows another embodiment of a stereo demultiplexer according to
5   the prior art; and

   Fig. 5   shows a further embodiment of a stereo demultiplexer according to
                  the prior art.

10 Fig. 1 shows a stereo demultiplexer according to a preferred embodiment of the
   present invention which elucidates the sampling rate decimation. As men-
   tioned above, such a sampling rate decimation according to the present inven-
   tion can be performed, because the frequency modulated stereo-multiplex sig-
   nal $m(t)$ has a much higher bandwidth than the frequency demodulated and
15 stereo-demultiplexed audio signal.

   As it is shown in Fig. 1, according to the present invention the stereo-sum sig-
   nal $m_s(t)$ is generated from the stereo-multiplex signal $m(t)$ by a sampling rate
   decimation with a decimation factor D by a first sampling rate decimation filter
20 5 which includes a lowpass filter.

   The so generated stereo-sum signal $m_s(t)$ is thereafter fed to an adder 3 and a
   subtracter 6 as described in connection with the stereo demultiplexers shown
   in Figs. 3 to 5.
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   According to the present invention also a digital PLL-circuit 4 is working with
   a decimated sampling rate, but the decimation filtering of the sum path, i.e.
   the path to generate the stereo-sum signal $m_s(t)$ is used for the sampling rate
   decimation of the stereo-sum signal $m_s(t)$ and the pilot carrier, i.e. the output
30 signal of the first sampling rate decimation filter 5 is not only input to the ad-
   der 3 and the subtracter 6, but also to the DPLL-cicrcuit 4.

   In the shown embodiment, the DPLL-circuit 4 generates a carrier for the coher-
   ent amplitude demodulation of the stereo-difference signal $m_d(t)$.
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   As also mentioned above, the coherent amplitude demodulation of the stereo-
   difference signal $m_d(t)$ needs to be performed at a sampling rate which is

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1   higher than the sampling rate of the audio signal, since the bandwidth of the
stereo-multiplex signal m(t) is higher than the bandwidth of the audio signal.
Therefore, the carrier for the coherent amplitude demodulation of the stereo-
difference signal $m_d(t)$ needs to be generated with a higher sampling rate. Fig.

5   1 shows that the carrier is generated with a sampling rate that is D times
higher than the sampling rate of the stereo-sum signal $m_s(t)$, since the second
harmonic of the pilot carrier generated by the DPLL-circuit 4 is interpolated by
an interpolation factor of D within the DPLL-circuit 4.

10 To perform the coherent amplitude demodulation which is necessary to gener-
ate the stereo-difference signal $m_d(t)$ the so generated carrier with a carrier fre-
quency of $2\omega_{pil}$ that is locked in phase to the pilot carrier is multiplied with the
stereo-multiplex signal m(t) by a demodulator 1 which directly corresponds to
the demodulators 1 described in connection with Figs. 3 to 5.

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The stereo-difference signal $m_d(t)$ is generated equally as described in connec-
tion with Figs. 3 to 5. Therefore, the output signal of the demodulator 1 is
sampling rate decimated by a second sampling rate decimation filter 2 which
includes a lowpass filter. The so generated stereo-difference signal $m_d(t)$ is fed

20 to an adder 3 and a subtracter 6 as described in connection with the stereo
demultiplexers described above in connection with Figs. 3 to 5.

Furtheron, if neccessary, delay elements which equalize the group delay of the
first and second sampling rate decimation filters in the sum path and the dif-

25 ference path can be inserted into the stereo-demiultiplexer to achieve that cer-
tain signals have the same time relationship.

Additionally to the usage of the decimation filtering of the sum path for the
sampling rate decimation of the pilot carrier a further sampling rate decima-

30 tion can be performed, e.g by a decimation factor of E. In this case also the in-
terpolation factor has to be increased to a value D·E, i.e. so that the recovered
pilot carrier has a sampling rate equal to that of the frequency demodulated
stereo-multiplex signal m(t).

35 Fig. 2 shows parts of the digital PLL-circuit 4 in more detail. Basically, the
digital PLL-circuit 4 comprises a PLL which outputs a phase signal, a
multiplier 13 which multiplies this phase signal with a constant factor which
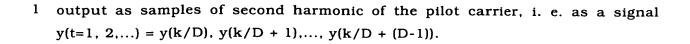
1 determines which harmonic of the pilot carrier is to be generated and one or
more sinus calculation units which output samples of the reconstructed pilot
carrier based on the multiplied phase signal. The number of sinus calculation
units determines the interpolation factor.

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The PLL itself comprises a first multiplier 7 receiving samples of the stereo-
sum signal $m_s(t=1, 2,...) = x(k)$ as multiplicant at a first input, a filter 8 receiv-
ing the output signal of said first multiplier 7, a second multiplier 9 multiply-
ing the output signal of the filter 8 with the gain of the phase locked loop, i. e.

10 with a signal PLL_loop_gain, a first adder 11 receiving said output signal of the
second multiplier 9 at a first input as a first summand, a constant represent-
ing the product of the pilot carrier frequency ω_{pil} and the sampling period T at
a second input as a second summand and a delayed phase signal which is the
output signal of said first adder 11 at a third input as a third summand, a de-

15 lay element 12 receiving said phase signal output of said first adder 11 and
supplying said delayed phase signal of said first adder 11 to said third input of
said first adder 11, and a cosinus calculation unit 10 receiving the phase sig-
nal of said first adder 11 and supplying its output signal as multiplier to a
second input of said first multiplier 7.

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To generate the second harmonic of the pilot carrier the phase signal is
multiplied with the constant factor 2 by the third multiplier 13. The output
signal of the third multiplier 13 is input to a first sinus calculation unit 14
which transfers the phase signal into a corresponding calculated sample of the

25 second harmonic of the pilot carrier.

To perform an interpolation with an interpolation factor D there is the need
that D-1 output samples are aditionally generated based on the phase signal
calculated on basis of one input sample x(k). Therefore, one of D-1 phase shift

30 values equally dividing the range to the next expected phase signal, i. e. the
phase signal for the input sample x(k+1), is respectively added to the phase
signal by a respective one of D-1 adders 16_1 to 16_{D-1} before these generated D-
1 phase signals are respectively input to D-1 sinus calculation units 15_1 to
15_{D-1}. These D-1 sinus calculation units respectively output one of D-1 inter-

35 polated samples of the second harmonic of the pilot carrier.

The output signals of the first to D^{th} sinus calculation units are sequentially

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1   output as samples of second harmonic of the pilot carrier, i. e. as a signal $y(t=1, 2,...) = y(k/D), y(k/D + 1),..., y(k/D + (D-1))$.

The cosinus calculation unit 10 and the sinus calculation units 14, 15_1 to 15_{D-1}
5   are advantageously realized as look-up tables. Of course, all sinus calculation units 14, 15_1 to 15_{D-1} can be realized as just one sinus calculation unit, since the respective output values are not needed simultaneously.

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